REMARKS

This is in response to the Office Action dated April 18, 2006. Examiner provisionally rejected claims 1-35 (all the claims) on the ground of nonstatutory obviousness-type double patenting as being unpatentable over certain claims of copending application serial number 10/029,709, hereinafter "709". In response to this rejection, Applicants are submitting a Terminal Disclaimer herewith.

Examiner rejected Claims 1-16 under 35USC112, second paragraph. Applicants have amended the claims to overcome this rejection.

Examiner also rejected all the claims 1-35, under 35 USC 103(a) as being unpatentable over Applicant Admitted prior Art, hereinafter "AAPA" in view of Kaylani et al (WO 00/46949), hereinafter "Kaylani". Applicants respectfully traverse this rejection and respectfully request favorable reconsideration in view of the comments set forth herein.

Examiner's rejection of Claim 1 (*see para. 8 of the Office Action)* is as follows: "As to claim 1, AAPA discloses a PLL/DLL dual loop data synchronous system comprising a phase lock loop (PLL), including a phase frequency detector (PFD) *403* receiving a local clock, a voltage controlled oscillator (VCO) *414*, a loop filter *412* coupled to said PFD and to said VCO, said loop filter configured to suppress VCO phase noise, and a phase shifter *409* coupled to said VCO and configured in a feedback loop with said PFD, etc." Note that in the foregoing quote from the Office Action, reference numerals have been added from FIG. 4 of the instant application, presumably the referenced AAPA. The portion of the Office Action that has been underlined is the portion of claim 1 that is not shown in FIG. 4 (Prior Art).

For purposes of this discussion, Examiner's rejection of Claim 1 (*see para. 8 of the Office Action)* is reproduced again; however, this time the reference numerals (with a somewhat stretched interpretation from FIG. 3 of Kaylani, as follows: "As to claim 1, AAPA discloses a PLL/DLL dual loop data synchronous system comprising a phase lock loop (PLL), including a phase frequency detector (PFD) *28* receiving a local clock,

a voltage controlled oscillator (VCO) *34*, a loop filter *32* coupled to said PFD and to sad VCO, said loop filter configured to suppress VCO phase noise, and a phase shifter *36* coupled to said VCO and configured in a feedback loop with said PFD, etc." The portion of the Office Action that has been underlined is the portion of claim 1 that is not shown in FIG. 3 of Kaylani.

The reason for the foregoing two paragraphs is to point out that neither of the two references teaches the structure, mode of operation and result claimed by Applicants. Both the AAPA reference and the Kaylani references use the same known approach in which the loop filter is NOT configured in a feedback loop with said PFD. Then, even if, *arguendo,* the output 42 (FIG. 3) in Kaylani were somehow fed back to Voltage Controlled Oscillator 34, this would provide the phase shifter "outside" the loop. Even with this hypothetical "outside" loop, Kaylani's design would be a cascade of loops. This means that the two loops would be sequential in nature. The PLL synthesizes a clock close to the correct frequency, then the DLL locks it to the desired frequency to match the data rate. In such a cascade of two loops, the second loop filters the jitter of the first loop, but the additive jitter of the second loop is unfiltered.

In contradistinction, Applicants' phase shifter is "inside" the loop. Applicants' claimed invention is a PLL/DLL dual loop data synchronization system in which the two loops interact so that the additive jitter of the PLL and DLL are filtered by both loops. This is a clearly patentable distinction as it is a feature neither taught nor suggested by either reference. When neither of two references teaches Applicants' invention then the combination of two such references cannot raise a question of obviousness under 35USC103. Accordingly, claim 1 is believed to be allowable. Claims 2-9 depend from claim 1 and are believed to be allowable for the same reasons and that they recite additional features of patentable import. Since dependent claims 2-9 are believed to depend from an allowable claim, no further discussion is warranted at this time.

Claim 10 was rejected in the Office Action (*see para. 11*) "for the same reasons as claim 1. In addition, AAPA discloses detecting a local reference at a PDF of a PLL (Fig. 5). Kaylani, however, filters a signal representative of a fill level of the FIFO (state of the FIFO, page 1, line 31." As was explained in connection with the structural

distinctions in claim 1, the method describedin claim 10 is similarly neither suggested nor taught by the Prior Art. For a more complete explanation, claim 10 is here reproduced as follows:

A method for PLL/DLL data serialization comprising:

detecting a local reference at a phase/frequency detector (PFD) of a phase lock loop (PLL);

phase locking a voltage controlled oscillator (VCO) of said PLL to a local reference to suppress a phase noise of said VCO;

receiving a parallel data input and a data clock at a FIFO register;

filtering, at a delayed lock loop (DLL), a signal representative of a fill level of said FIFO;

phase shifting an output of said VCO of said PLL in response to said filtering step;

locking said PLL to a frequency corresponding to a pre-filtered signal input to said DLL;

receiving, at a parallel-in serial-out (PISO) serializer, said parallel data and said VCO output; and

outputting a serialized data from said PISO serializer with said VCO output a transmit clock.

The underlined method steps cannot be found in the prior art of record. As noted hereinabove, in Applicants' embodiment, the PLL and DLL are filtered in both loops in accordance with the combination of method steps set forth in claim 10. Accordingly, claim 10 is believed to be allowable. Claims 11-16 dependent in various ways from claim 10 are believed to be allowable for the same reasons and also because they recite additional features. Since claims 11-16 depend from an allowable claim, no additional discussion with respect to these claims is warranted.

In the Office Action, (*see paragraph 12*), "claims 17, 23 and 29 are rejected for the same reasons as claim 1, etc". Regarding claim 17, there is recited: a phase shifter configured in a

feedback loop with said PFD within said PLL. This is the same feature relied on for the patentability of claim 1 (in the overall combination) and is equally applicable to the combination recited in claim 17. Accordingly, claim 17 is believed to be allowable for the same reasons as claim 1. Claims 18-22, dependent in various degrees on claim 17 are believed to be allowable because they depend from an allowable claim and also because they recite additional features. No further discussion of claims 18-22 appears warranted.

Regarding claim 23, the patentable import is best understood by reproducing the claim, as follows:

A plesiochronous data retiming method comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

deserializing said serial data to a parallel data using said recovered clock;

writing said parallel data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading said parallel data from said FIFO;

serializing said parallel data using said synthesized transmit clock;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

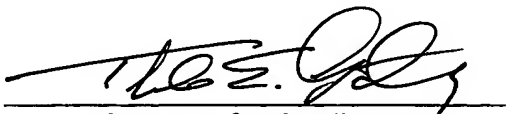
Neither the AAPA nor the Kaylani reference teach the claimed series of method steps and in particular the underlined portions of claim 23. As noted in connection with claim 1, in Applicants' embodiment the DLL and PLL loops interact so that the additive jitter is filtered by both loops. This is a concept envisioned by neither of the currently cited references. Accordingly, claim 23 is believed to recite patentable subject matter. Since claim 23 is believed to be allowable, dependent claims 24-28 are believed to be allowable for the same reasons and as

they recite additional features. No further discussion of claims 24-28 appears required for establishing their patentability.

Claim 29 was rejected in paragraph 12 of the Office Action for the same reasons as claim 1, as well as additional reasons. Since claim 1 is now believed to be allowable, that portion of the rejection is believed to have been overcome. In addition, as noted with respect to claim 23, claim 29 recites, in part: detecting a FIFO fill level at a delay locked loop (DLL); and phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step. Accordingly, claim 29 should be allowed for the same reasons as claims 1 and 23. Dependent claims 30-35 should be allowed for the same reasons as claim 29 because they depend from claim 29 and that they recite additional features. No further discussion of claims 30-35 appears to be required.

In view of the foregoing, claims 1-35, i.e. all the claims in this application are believed to be in condition for allowance. Examiner is respectfully requested to telephone the undersigned if there is a question or if such would further the prosecution of this application. An early notification of allowance is earnestly solicited.

Respectfully submitted,
Benjamim TANG et al



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